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ABSTRACT

A method of fabricating a semiconductor device including providing a semiconductor heterostructure, the heterostructure having a relaxed $Si_{1-x}Ge_x$ layer on a substrate, a strained channel layer on the relaxed $Si_{1-x}Ge_x$ layer, and a $Si_{1-y}Ge_y$ layer; removing the $Si_{1-y}Ge_y$ layer; and providing a dielectric layer. The dielectric layer includes a gate dielectric of a MISFET. In alternative embodiments, the heterostructure includes a SiGe spacer layer and a Si layer.